

Development of Low Cost Millimeter Wave MMIC

Koji TSUKASHIMA*, Miki KUBOTA, Osamu BABA, Hideki TANGO, Atsushi YONAMINE, Tsuneo TOKUMITSU and Yuichi HASEGAWA

This paper describes the cost effective 77 GHz transmitter and receiver MMIC (monolithic microwave integrated circuit) that uses a three-dimensional MMIC technology optimized for flip-chip implementation. The MMIC structure incorporates inverse TFMS lines so that a ground metal can be applied to cover the whole chip surface except for interconnect pads. Four metal layers, each of them are covered with polyimide and SiN films. Hence, these MMIC chips require no package, and can be directly assembled on a printed circuit board. The transmitter MMIC is composed of an x8 multiplier chain (9.5 GHz/38 GHz MLT, 38 GHz AMP, and 38 GHz/76 GHz MLT), and a driver + power amplifier. A saturated output power of 14 dBm has been obtained between 76 and 77 GHz from this transmitter MMIC. A portion of the 38 GHz amplifier output is split for the receiver mixer. The receiver MMIC is composed of multi LNA + MIX blocks and a common x2 multiplier block that provides a 10 dBm of local oscillator power. A receiver gain of 10 dB and a noise figure of 7.8 dB for a baseband frequency at 10 MHz have been obtained. The die size of the transmitter is 1.5 mm x 2.0 mm and the chip area of the receiver is 1.9 mm x 1.3 mm.

Keywords: 3D-MMIC, WLCSP, automotive radar, transmitter, receiver

1. Introduction

Recently, SiGe (silicon germanium) HBT (heterojunction bipolar transistor) transceivers for automotive radar application have been gaining worldwide interests because of their low cost nature and full integration concept. The transmitter is composed of a VCO (voltage controlled oscillator) of 76 GHz band associated with a high-order prescaler^{(1),(2)}. The power amplifier is controlled at a stable output power level, in which no saturation operation is used. This development concept sounds very effective for large-scale production. However, its reliability and 77 GHz output power issues remain critical, and its complex full integration largely depends on radar system standardization. Yield degradation caused by high resolution process is also worried. The conventional GaAs (gallium arsenide) pHEMT (pseudomorphic high electron mobility transistor) approach remains in the main stream of the market, which is ever growing and far from saturation. SiGe HBT and CMOS (complementary metal oxide semiconductor) transceivers can be expected as future systems if these critical issues are solved.

Although mechanical beam scanning radar applications are still majority in the market, electronic beam steering is expected to be a major stream, where implementation of multiple receiver front-ends in a package or in an MMIC is essential.

We have been engaged in the development of a single-chip multiple-input receiver MMIC and a transmitter MMIC by incorporating GaAs three-dimensional MMIC technology⁽³⁾. There were two choices; one is a face-up structure, and the other is a flip-chip structure. The flip-chip structure can be very cost effective because, by employing inverse TFMS line-based circuit design and the surface ground plane, the MMICs can be solder-reflow-compatible SMT products, viz. WLCSP (wafer level chip size package). The three-dimensional MMIC we employ has four metal

layers, and, to make them humidity proof, SiN coating is applied to each polyimide layer.

In this paper, a transmitter MMIC (composed of a 9.5 GHz/76 GHz frequency multiplier chain, a driver amplifier, and a saturated power amplifier) and a receiver MMIC (composed of multi receiver front-ends and a common LO circuit) will be demonstrated. These CSP MMICs are realized in the areas of 3.0 and 2.47 mm².

2. WLCSP Structure and pHEMT

An SMT compatible WLCSP structure is shown in **Fig. 1**. Among multi-polyimide layers, four metal (Au) layers can be composed. This structure is same as that of our three-dimensional MMIC⁽³⁾, and additionally, is covered with common ground on the top (4th) metal layer, which is covered with a relatively thick polyimide/SiN films to form interconnects between MMIC and PCB (printed circuit board). A number of small-circle ground attaches are periodically formed on the common ground metal, increas-

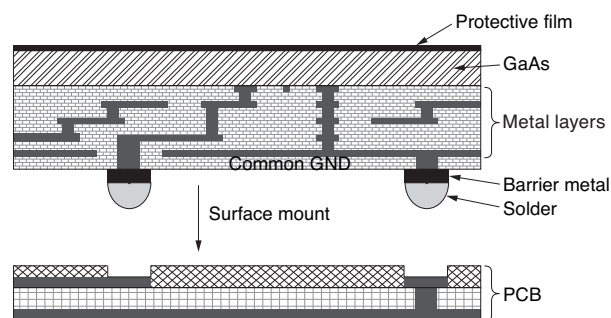


Fig. 1. Cross sectional view of WLCSP

ing both mechanical strength and parallel-plate mode suppression effects. This improves the SMT (surface mount technology) property⁽⁴⁾. Protective film is formed on the backside of die to eliminate troubles in chip mounting process. Strip conductors, as a signal line, are mainly formed on the first metal layer to minimize the transmission loss, and other-layer strips are used for effective layout formation. Hence, the incorporated transmission lines are inverse TFMS lines. The loss of 10 μm -width 50 Ω -line on the first metal layer is 1.1 dB/mm at 76 GHz. The active device process employs an AlGaAs/GaAs 0.10 μm pHEMT with an f_T of 85 GHz and an f_{max} of 230 GHz ($\text{NF}_{\text{min}} = 0.5$ dB at 12 GHz), MIM capacitors, and epitaxial resistors.

3. Transmitter MMIC

A transmitter block diagram is shown in Fig. 2, where main stuff is an amplifier and a frequency multiplier. A 9.5 GHz 10 dBm VCO output signal is assumed to be input to LO (local) port.

The current-reuse amplifier^{(3),(5)} is employed due to its high gain and small size features. The x8 frequency multiplication is performed by cascade-connecting a 9.5 GHz/38 GHz quadrupler and a 38 GHz/76 GHz doubler via a saturated 38 GHz amplifier stage. The circuit scheme is shown in Fig. 3. Each multiplier (x4 and x2) incorporates a balanced topology⁽⁶⁾ that combines a common-gate-

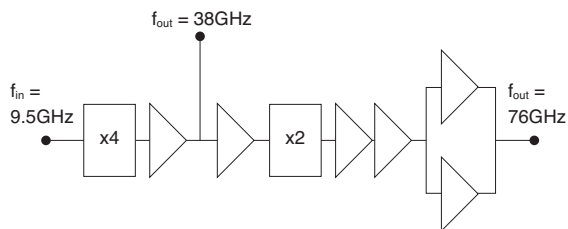


Fig. 2. Employed transmitter configuration

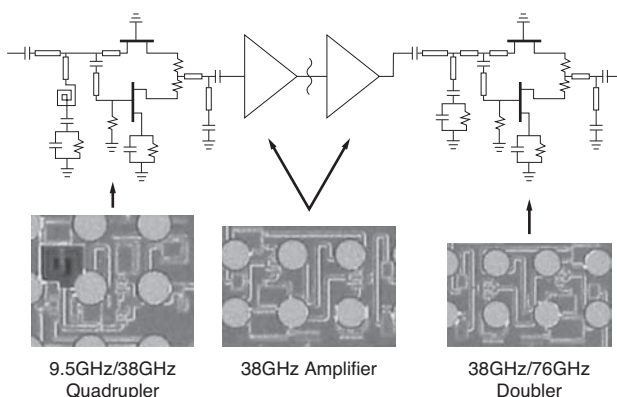
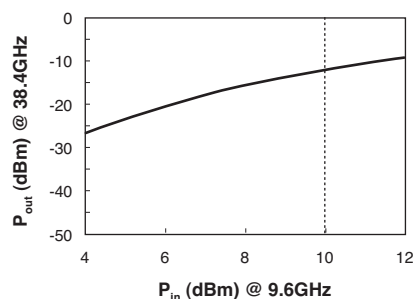
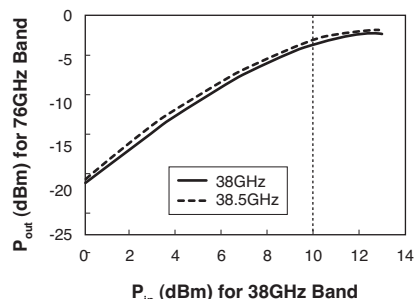


Fig. 3. Designed multiplier (x8) chain scheme and fabricated chain components

HEMT and a common-source-HEMT in parallel. This topology is wideband (for example, 34-40 GHz for the quadrupler) and very suitable to minimize the circuit area, performance variation with temperature, and transmission of the third harmonic signals. Additionally, because the input impedance of the pair of HEMTs is as low as nearly 50 Ω , the injection power level can be increased without damaging the gate contact. This further stabilizes the output power level. Between the quadrupler and the doubler, a 2-stage 38 GHz current-reuse saturated amplifier is incorporated to minimize the variation of 77 GHz output power from the doubler. The amplifiers are identical and also serve as band-pass filters. When the power supply to the x8 multiplier chain is 5 V, the current is less than 70 mA. The frequency conversion characteristics of the quadrupler and doubler are shown in Fig. 4. The values of the conversion loss of the multipliers are 22 dB and 13 dB, where the input signal level is set at nearly 10 dBm.



(a) 9.5 GHz/38 GHz quadrupler



(b) 38 GHz/76 GHz doubler

Fig. 4. Measured performance of the quadrupler and doubler

The power amplifier consists of two amplifiers connected in parallel by Wilkinson dividers, and follows the two-stage driver amplifiers. The gate size of each amplifier is 40 μm x 4 fingers. The unit amplifier employs a current-reuse topology (same as that of the 38 GHz amplifier) for high gain and quick saturation response due to halved drain-source voltage⁽³⁾. The Wilkinson divider occupies a small area because the line-to-line spacing can be as narrow as 30 μm with negligibly small coupling. The gain and the saturated output power level for each unit amplifier are 11 dB and 10 dBm respectively. Measured small-signal per-

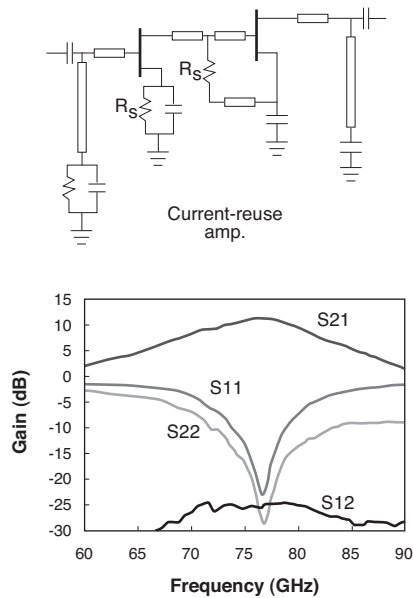
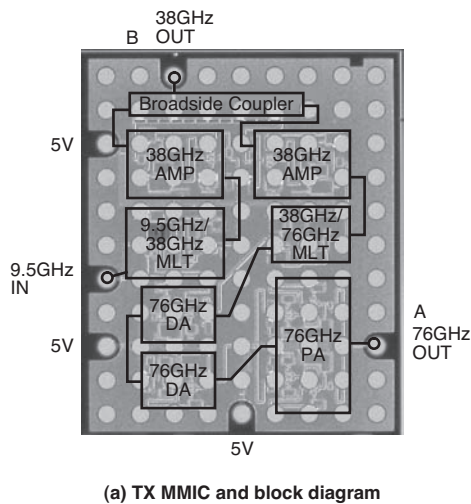
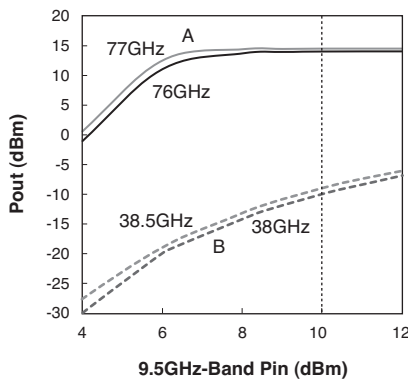


Fig. 5. Measured small-signal performance of a unit amplifier



(a) TX MMIC and block diagram



(b) Measured conversion performance

Fig. 6. TX MMIC and its measured output power performance

formance of the unit amplifier is shown in Fig. 5.

A die photograph and the measured total performance of a TX (transmitter) MMIC shown in Fig. 2 are demonstrated in Fig. 6. The performance was measured with use of on-wafer probes. The compact and well-arranged layout of components mitigated the die size restriction. The die size was 1.5 mm x 2.0 mm. The saturated output power level was 14 dBm for a 9.5 GHz-band 10 dBm input. When the half-frequency component was measured at a level 20 dB lower than that of the 76 GHz-band component, the other half was rejected by the waveguide-to-antenna interface. A 38 GHz output port is prepared for the RX (receiver) MMIC's LO input. This TX MMIC consumes 650 mW (5 V, 130 mA).

4. Receiver MMIC

A receiver block diagram is shown in Fig. 7, where two low-noise front-end units and a common LO circuitry are integrated. Each front-end unit is composed of a two-stage LNA and a balanced resistive mixer. A 38 GHz/76 GHz doubler and associated amplifiers supply a 10 dBm of 76 GHz-band LO signal to the mixers. In the RX MMIC design, the LO port frequency is chosen to be 38 GHz to remove any instability and oscillation around the 76 GHz band. The TX MMIC also provides a pair of 38 GHz output ports (-2 dBm) due to the same reason. Hence, a common 38 GHz/76 GHz doubler chain is designed and implemented so as to reduce the size of RX MMIC. The amplifier topology is the same as that of the TX MMIC. As for the LNA, the gate size is $40 \mu\text{m} \times 2$ fingers, and the drain current is adjusted for lower noise figure.

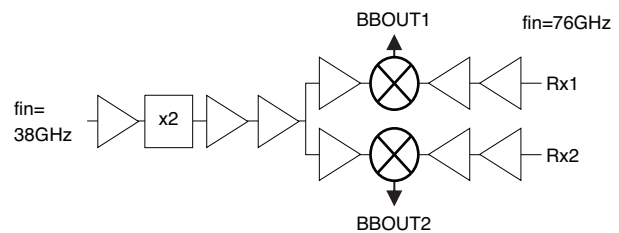


Fig. 7. Employed two-channel receiver configuration

The balanced resistive mixer is temperature insensitive (less than 1 dB in the operating temperature) and has a high IP1dB performance (nearly 5 dBm). The conversion loss is nearly 12 dB. Its DC bias-less scheme reduces power consumption by the mixer. The mixer topology with LO-RF (radio frequency) leakage suppression and the performance are shown in Fig. 8.

A chip photograph and the measured total performance of the RX MMIC are demonstrated in Fig. 9. The performance is measured with use of on-wafer probes. This RX MMIC is also compactly arranged to be installed to a small

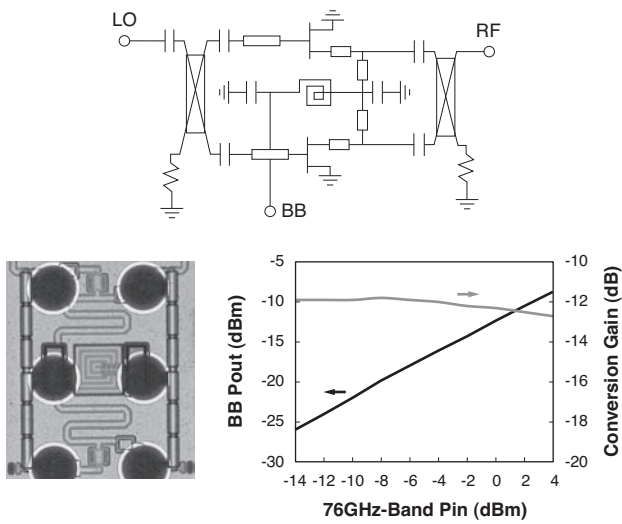
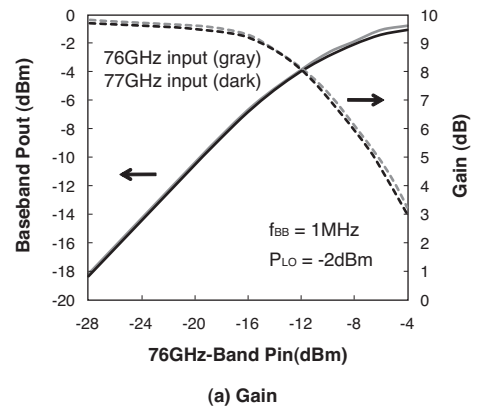
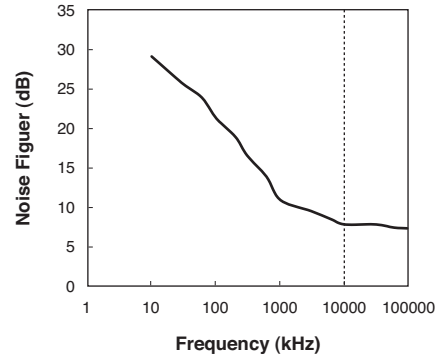


Fig. 8. Balanced resistive mixer and its performance



(a) Gain



(b) Baseband noise figure

Fig. 10. Measured performances of RX MMIC

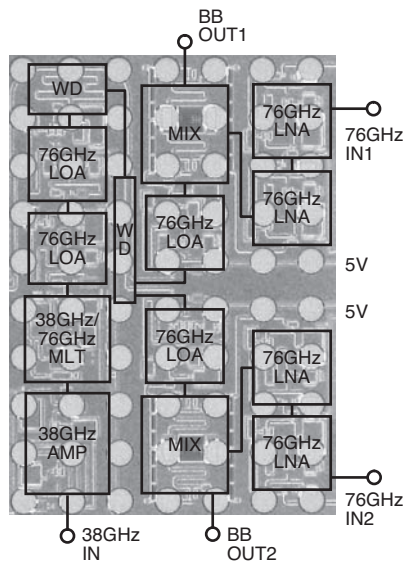


Fig. 9. RX MMIC and block diagram

chip area. The chip area is 1.9 mm x 1.3 mm. The measured gain and noise figure performance are shown in Fig. 10. The linear gain is nearly 10 dB, and the IP1dB (input 1 dB compression point) is -14 dBm. The noise figure curve exhibits -10 dB/decade below 1 MHz, reaching 7.8 dB at 10 MHz, where the power consumption is 500 mW (5 V, 100 mA).

An important issue for the RX MMIC is the isolation among the multiple 76 GHz-band input ports. It is not reasonable to measure the port isolation characteristics for face-up setup, because the circuitry is sandwiched by two metals; one is the surface ground metal of the die and the other is a metal plate for a measurement setup. To verify realistic isolation characteristics, a test board designed for flip-chip implementation is necessary. With our newest test

board, we confirmed an isolation of greater than 35 dB. Although further improvement is required for the die and radar module measurements, the TX MMIC outputs 13.5 dBm when implemented on this test board.

5. Conclusions

Transmitter and receiver MMICs using WLCSP technology have been developed. These are integrated in small chips of 1.5 mm x 2.0 mm and 1.9 mm x 1.3 mm respectively. The saturated output power of the transmitter MMIC is 14 dBm at 76-77 GHz, while the receiver MMIC exhibits the gain of 10 dB and noise figure of 7.8 dB for a baseband frequency at 10 MHz. We believe that this development will be a solution for further cost reduction of automotive radar devices.

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Contributors (The lead author is indicated by an asterisk (*)).

K. TSUKASHIMA*

- Advanced Circuit Design R&D Department, Transmission Device R&D Laboratories

He is engaged in the research and development of millimeter wave MMICs.



M. KUBOTA

- Manager, Advanced Circuit Design R&D Department, Transmission Device R&D Laboratories

O. BABA

- Assistant Manager, Advanced Circuit Design R&D Department, Transmission Device R&D Laboratories

H. TANGO

- Assistant Manager, Radio Transmission Systems Department, Information & Communications Laboratories

A. YONAMINE

- Advanced Circuit Design R&D Department, Transmission Device R&D Laboratories

T. TOKUMITSU

- Ph.D.
IEEE Fellow
Chief Engineer, Transmission Device R&D Laboratories

Y. HASEGAWA

- Sumitomo Electric Device Innovations, Inc.